



+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

MAX3840

General Description

The MAX3840 is a dual 2 × 2 asynchronous crosspoint switch for SDH/SONET DWDM and other high-speed data switching applications where serial data stream loop-through and protection channel switching are required. It is ideal for OC-48 systems with forward error correction. A high-bandwidth, fully differential signal path minimizes jitter accumulation, crosstalk, and signal skew. Each 2 × 2 crosspoint switch can fan out and/or multiplex up to 2.7Gbps data and 2.7GHz clock signals. All inputs and outputs are current mode logic (CML) compatible and easily adaptable to interface with an AC-coupled LVPECL signal. When not used, each CML output stage can be powered down with an enable control to conserve power. The typical power consumption is 460mW with all outputs enabled.

The MAX3840 is compatible with the MAX3876 2.5Gbps clock and data recovery (CDR) circuit.

The MAX3840 is available in a 32-pin exposed-pad QFN package (5mm × 5mm footprint) and operates from a +3.3V supply over a temperature range of -40°C to +85°C.

Applications

SDH/SONET and DWDM Transport Systems
 Add-Drop Multiplexers
 ATM Switch Cores
 WDM Cross-Connects
 High-Speed Backplanes

Features

- ◆ Single +3.3V Supply
- ◆ 460mW Power Consumption
- ◆ 2ps_{RMS} Random Jitter
- ◆ 7psp-p Deterministic Jitter
- ◆ Power-Down Feature for Deselected Outputs
- ◆ CML Inputs/Outputs
- ◆ 6ps Channel-to-Channel Skew
- ◆ 100ps Output Edge Speed
- ◆ 5mm × 5mm 32 QFN or Thin QFN Package

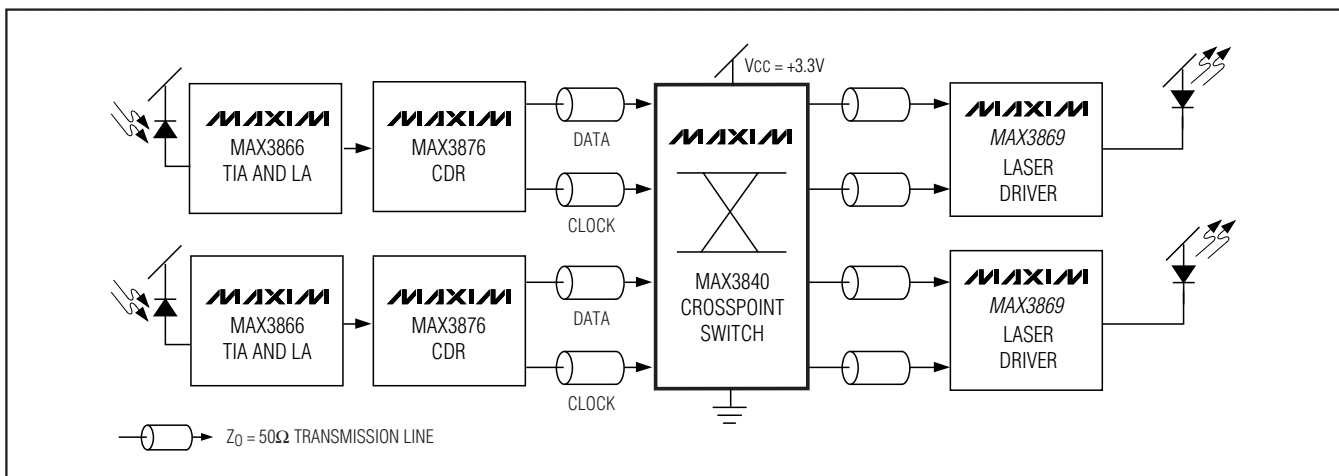
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3840ETJ+	-40°C to +85°C	32 TQFN	T3255-3
MAX3840EGJ	-40°C to +85°C	32 QFN	G3255-1

+Denotes lead-free package.

Pin Configurations appear at end of data sheet.

Typical Application Circuit



+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} -0.5V to +5.0V
 Input Voltage (CML)($V_{CC} - 1.0$) to ($V_{CC} + 0.5$ V)
 TTL Control Input Voltage.....-0.5V to ($V_{CC} + 0.5$ V)
 Output Currents (CML)22mA
 Continuous Power Dissipation ($T_A = +85^\circ\text{C}$)
 32-Pin TQFN
 32-Pin QFN
 (derate 21.3mW/ $^\circ\text{C}$ above +85 $^\circ\text{C}$).....1.38W

32-Pin QFN
 (derate 21.3mW/ $^\circ\text{C}$ above +85 $^\circ\text{C}$).....1.38W
 Operating Temperature Range-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
 Operating Junction Temperature Range.....-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
 Storage Temperature Range-65 $^\circ\text{C}$ to +160 $^\circ\text{C}$
 Lead Temperature (soldering, 10s).....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0\text{V}$ to +3.6V, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$. Typical values are at $V_{CC} = +3.3\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	All outputs enabled		140	190	mA
CML INPUT AND OUTPUT SPECIFICATIONS						
CML Differential Output Swing		$R_L = 50\Omega$ to V_{CC} (Figure 2)	640	800	1000	mV _{P-P}
Differential Output Impedance			85	100	115	Ω
CML Output Common-Mode Voltage		$R_L = 50\Omega$ to V_{CC}		$V_{CC} - 0.2$		V
CML Single-Ended Input Voltage Range	V_{IS}		$V_{CC} - 0.8$		$V_{CC} + 0.4$	V
CML Differential Input Voltage Swing			300		1600	mV _{P-P}
CML Single-Ended Input Impedance			42.5	50	57.5	Ω
TTL SPECIFICATIONS						
TTL Input High Voltage	V_{IH}		2.0			V
TTL Input Low Voltage	V_{IL}				0.8	V
TTL Input High Current	I_{IH}		-10		+10	μA
TTL Input Low Current	I_{IL}		-10		+10	μA

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

MAX3840

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CML Input and Output Data Rate				2.7		Gbps
CML Input and Output Clock Rate				2.7		GHz
CML Output Rise and Fall Time	t_r, t_f	20% to 80%		100	136	ps
CML Output Random Jitter	RJ	(Note 2)		2		psRMS
CML Output Deterministic Jitter	DJ	(Note 3)		7	20	ps _{P-P}
CML Output Differential Skew	t_{skew1}	Any differential pair		7	25	ps
CML Output Channel-to-Channel Skew	t_{skew2}	Any two outputs		15	40	ps
Propagation Delay from Input-to-Output	t_d			185		ps

Note 1: AC characteristics are guaranteed by design and characterization.

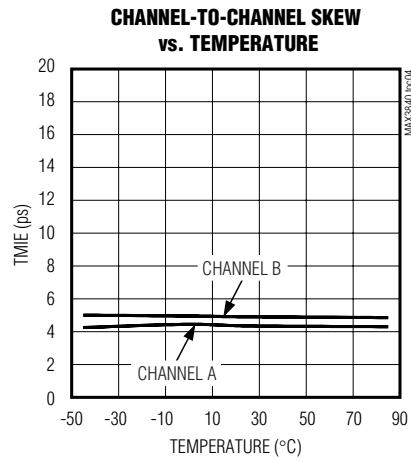
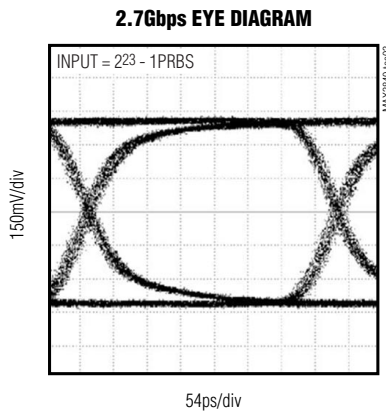
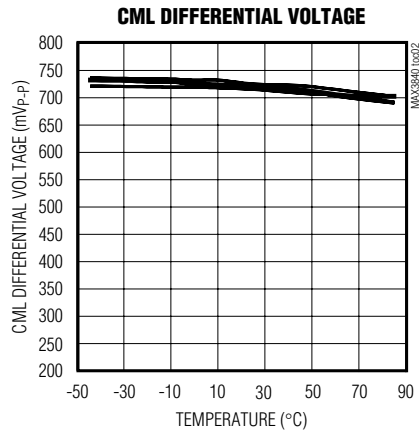
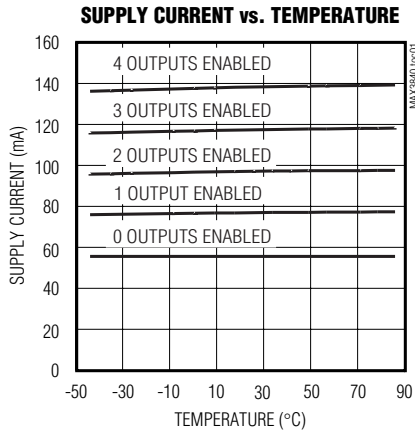
Note 2: Measured with 100mV_{P-P} noise ($f \leq 2MHz$) on the power supply.

Note 3: Deterministic jitter (DJ) is the arithmetic sum of pattern-dependent jitter and pulse width distortion.

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)



+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Pin Description

MAX3840

PIN	NAME	FUNCTION
1	ENB1	Channel B1 Output Enable, TTL Input. A TTL low input powers down B1 output stage.
2	DIB1+	Channel B1 Positive Signal Input, CML
3	DIB1-	Channel B1 Negative Signal Input, CML
4	ENB0	Channel B0 Output Enable, TTL Input. A TTL low input powers down B0 output stage.
5	SELB0	Channel B0 Output Select, TTL Input. See Table 1.
6	DIB0+	Channel B0 Positive Signal Input, CML
7	DIB0-	Channel B0 Negative Signal Input, CML
8	SELB1	Channel B1 Output Select, TTL Input. See Table 1.
9, 24	GND	Supply Ground
10, 13, 16, 17, 20, 23	V _{CC}	Positive Supply
11	DOB0-	Channel B0 Negative Output, CML
12	DOB0+	Channel B0 Positive Output, CML
14	DOB1-	Channel B1 Negative Output, CML
15	DOB1+	Channel B1 Positive Output, CML
18	DOA1-	Channel A1 Negative Output, CML
19	DOA1+	Channel A1 Positive Output, CML
21	DOA0-	Channel A0 Negative Output, CML
22	DOA0+	Channel A0 Positive Output, CML
25	SELA1	Channel A1 Output Select, TTL Input. See Table 1.
26	DIA0+	Channel A0 Positive Signal Input, CML
27	DIA0-	Channel A0 Negative Signal Input, CML
28	SELA0	Channel A0 Output Select, TTL Input. See Table 1.
29	ENA0	Channel A0 Output Enable, TTL Input. A TTL low input powers down A0 output stage.
30	DIA1+	Channel A1 Positive Signal Input, CML
31	DIA1-	Channel A1 Negative Signal Input, CML
32	ENA1	Channel A1 Output Enable, TTL Input. A TTL low input powers down A1 output stage.
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board ground for proper electrical and thermal operation.

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Table 1. Output Routing

ROUTING CONTROLS		OUTPUT CONTROLS		OUTPUT SIGNALS	
SELA0/SELB0	SELA1/SELB1	ENA0/ENA1	ENB0/ENB1	Signal at DOA0/DOB0	Signal at DOA1/DOB1
0	0	1	1	DIA0/DIB0	DIA0/DIB0
0	1	1	1	DIA0/DIB0	DIA1/DIB1
1	0	1	1	DIA1/DIB1	DIA0/DIB0
1	1	1	1	DIA1/DIB1	DIA1/DIB1
X	X	0	0	Power Down	Power Down

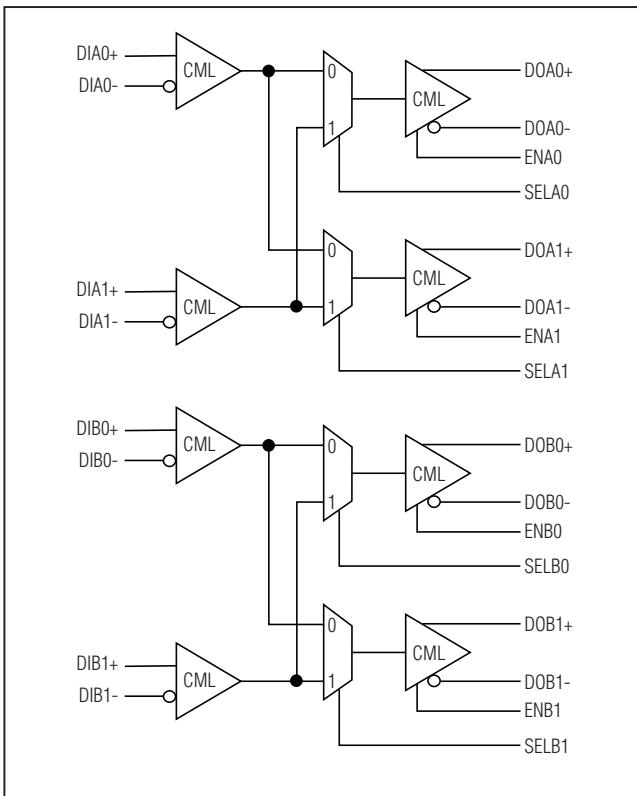


Figure 1. Functional Block Diagram

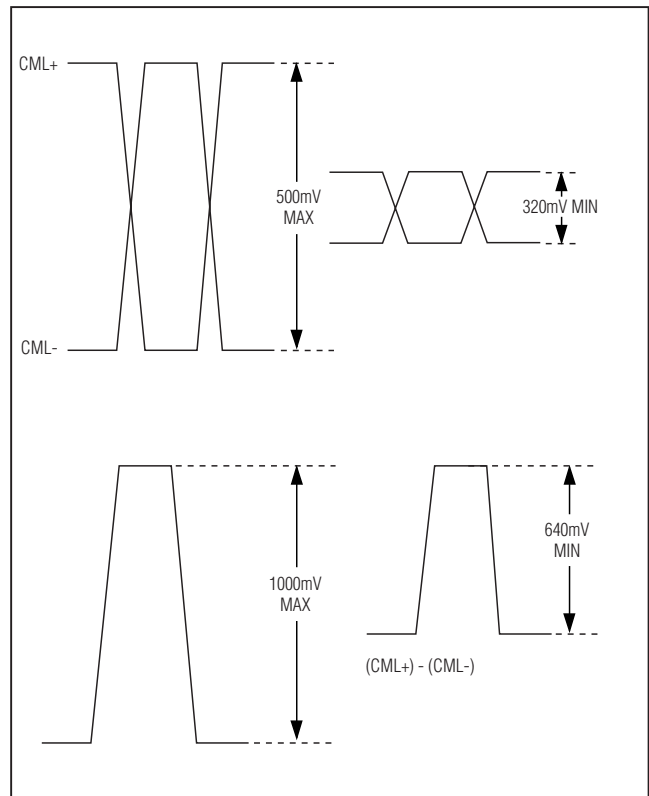


Figure 2. CML Output Levels

Detailed Description

The block diagram in Figure 1 shows the MAX3840 architecture. The SELA_ and SELB_ pins control the routing of the signals through the crosspoint switch. Each output of the crosspoint switch drives a CML output driver. Each of the outputs, DOA_ and DOB_, is enabled or disabled by the respective ENA_ and ENB_ pins.

CML Inputs and Outputs

CML is used to simplify high-speed interfacing. On-chip input and output terminations minimize the number of external components required while improving signal integrity. The CML output signal swing is small, resulting in lower power consumption. The internal 50Ω input and output terminations minimize reflections and eliminate the need for external terminations.

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Applications Information

Interfacing PECL Inputs and Outputs to the MAX3840

For information on interfacing with CML, refer to Maxim Application Note HFAN-01.0, *Introduction to LVDS, PECL, and CML*.

Layout Techniques

For best performance, use good high-frequency layout techniques, filter VCC supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3840 data inputs and outputs.

Interface Models

Figure 3 shows the interface model for the CML inputs, and Figure 4 shows the model for CML outputs.

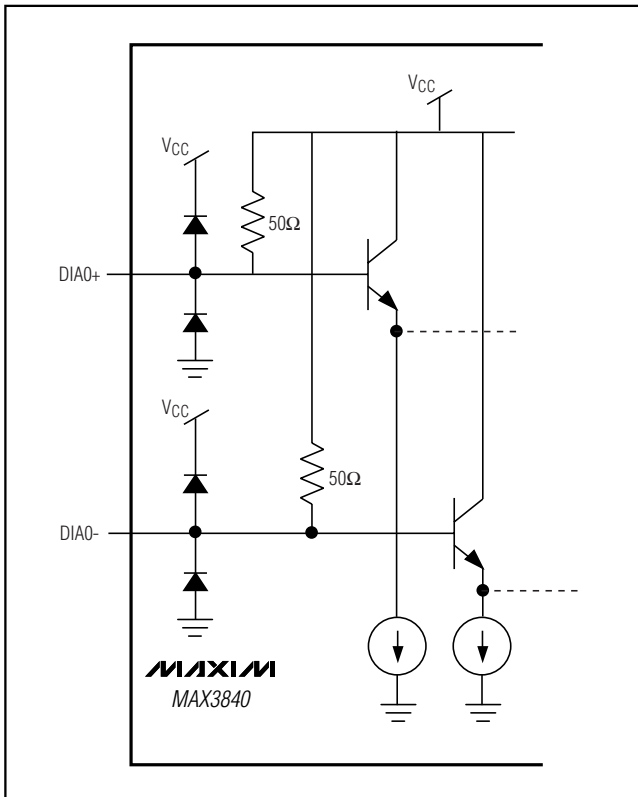


Figure 3. CML Input Model

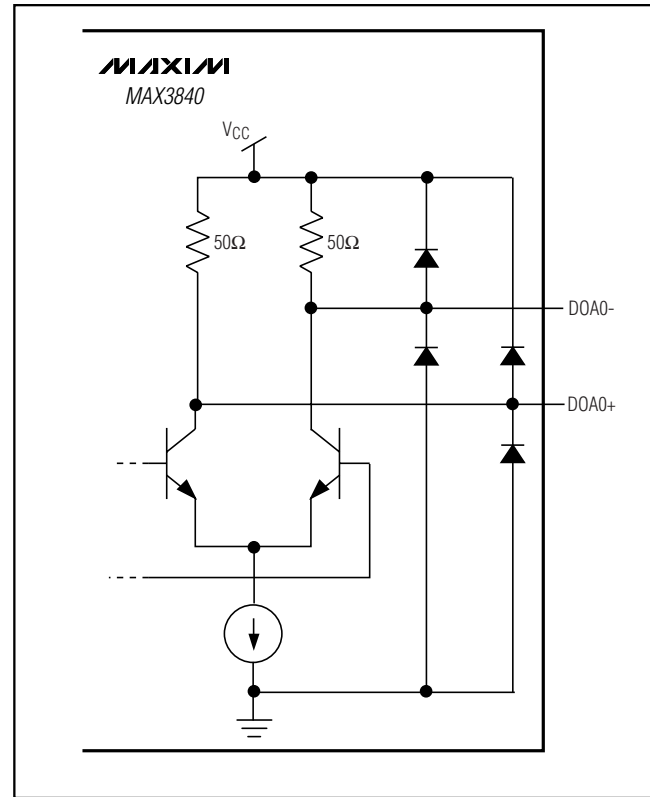
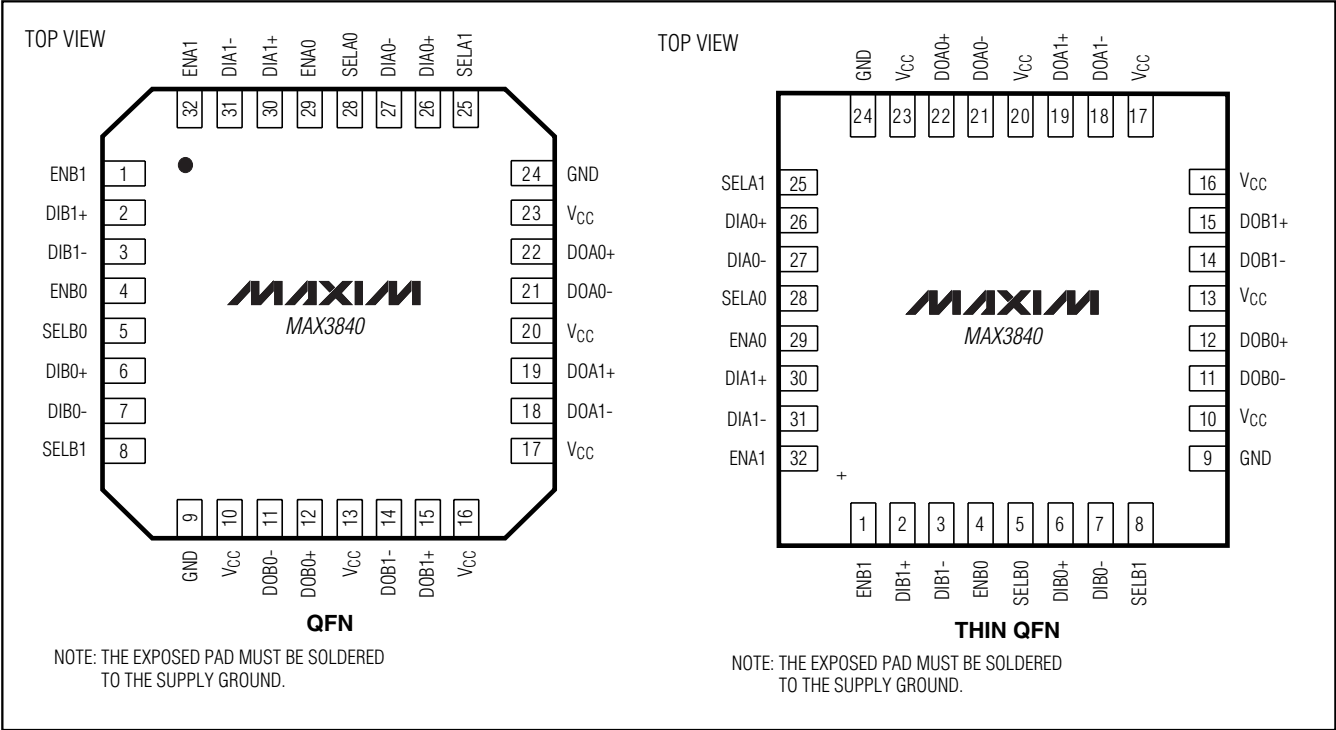


Figure 4. CML Output Model

MAX3840

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Pin Configurations



Chip Information

TRANSISTOR COUNT: 1200

PROCESS: Bipolar (SiGe)

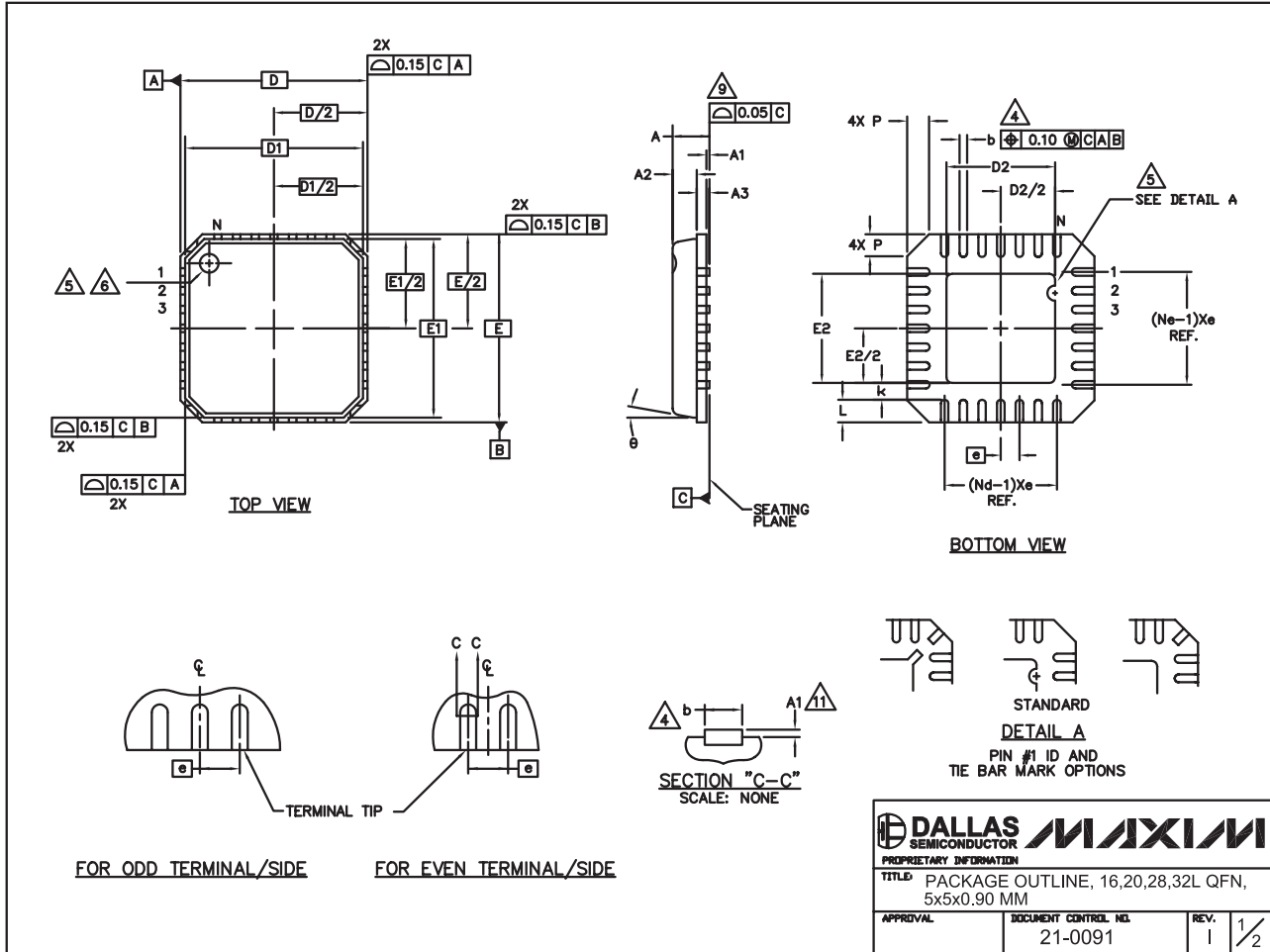
+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX3840

32L QFN, EPS



+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Package Information (continued)

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COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
ϕ	0"		12"	0"		12"	0"		12"	0"		12"

EXPOSED PAD VARIATIONS						
PKG CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.55	2.70	2.85	2.55	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.55	2.70	2.85	2.55	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

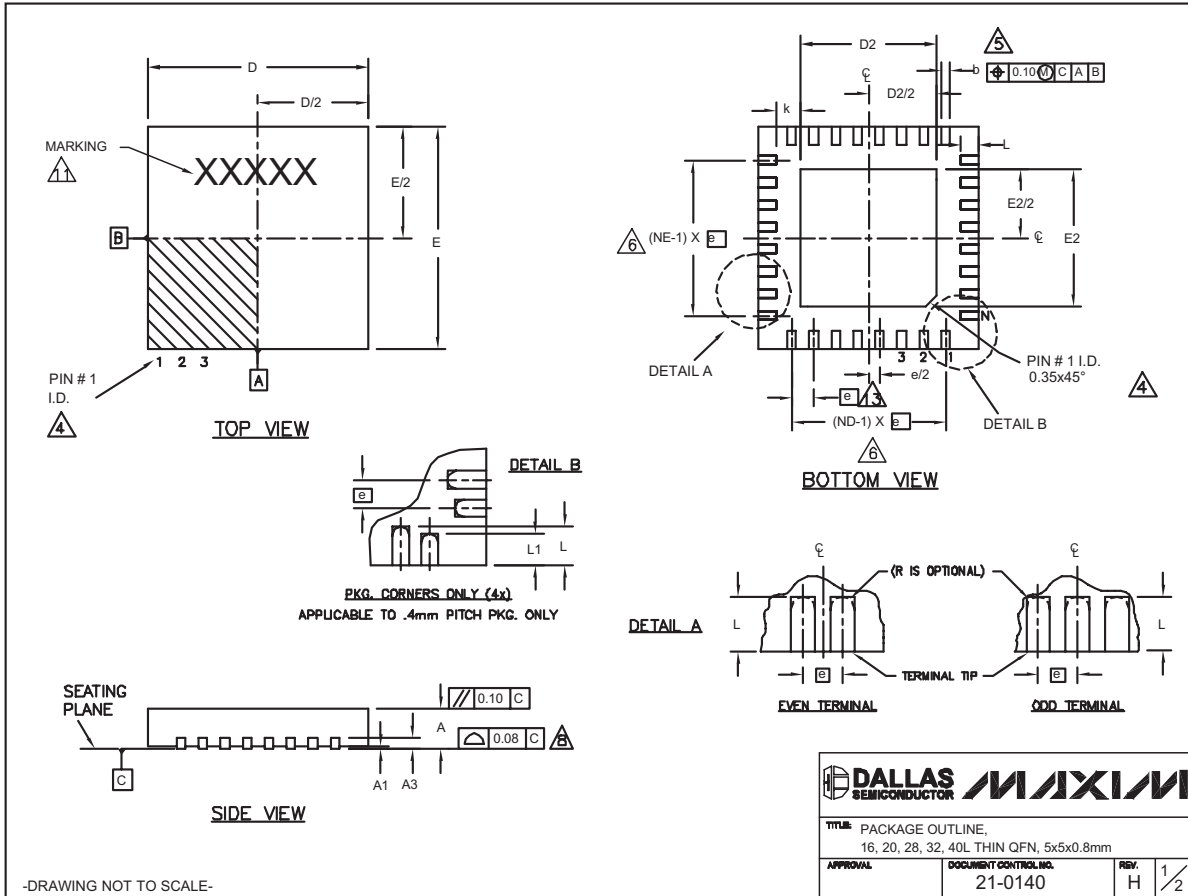
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. — 1994.
3. N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
12. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM		
APPROVAL	DOCUMENT CONTROL NO. 21-0091	REV. 1 2/2

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Package Information (continued)

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MAX3840

+3.3V, 2.7Gbps Dual 2 × 2 Crosspoint Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			----		

EXPOSED PAD VARIATIONS										
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES		
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES		
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES		
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO		
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO		
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES		
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES		
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO		
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO		
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES		
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES		
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO		
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES		
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO		
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES		

** SEE COMMON DIMENSIONS TABLE

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR		MAXIM	
TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	H	2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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